Supplementary Material of DrlGoFPGA

E. Comparison with OpenPARF

In TABLE VII, 'CIIs' are clock illegal instances. 'MVD' is the maximum violation distance in CIIs. 'AVD' is the average violation distance in CIIs. TABLE VII shows that compared to OpenPARF, DrlGoFPGA01-PT can reduce 3 CIIs in the global placement (GP) phase of the ISPD'2017 benchmarks. Although DrlGoFPGA01-PT increased MVD by 3.4 µm, it decreased AVD by 0.1 µm Therefore, DrlGoFPGA has an advantage in handling clock routing constraints during the GP optimization phase.

TABLE VII
CLOCK ROUTING CONSTRAINT ANALYSIS OF OPENPARF AND DRLGOFPGA IN THE GLOBAL PLACEMENT PHASE

Design	OpenPARF [4]			DrlGoFPGA01-PT		
	CIIs	MVD	AVD	CIIs	MVD	AVD
CLK-FPGA01	1	5.2	5.2	7	19.3	8.7
CLK-FPGA02	0	0	0	0	0	0
CLK-FPGA03	111	132.6	18.2	80	175.0	21.4
CLK-FPGA04	25	28.7	7.3	25	32.5	8.3
CLK-FPGA05	17	35.6	12.1	18	54.2	16.4
CLK-FPGA06	67	70.6	16.1	60	73.1	14.1
CLK-FPGA07	5	16.5	6.9	6	28.2	7.1
CLK-FPGA08	0	0	0	1	0.6	0.6
CLK-FPGA09	4	8.1	4.3	5	6.7	2.5
CLK-FPGA10	25	79.7	11.3	10	20.6	7.3
CLK-FPGA11	32	63.7	16.8	29	51.1	17.6
CLK-FPGA12	9	41.3	14.7	17	66.8	10.1
CLK-FPGA13	4	10.4	5.4	4	8.6	3.1
Avg.	23	37.9	9.1	20	41.3	9.0

DrlGoFPGA01-PT: During model testing, the GO method uses OpenPARF.

F. Comparison with OpenPARF 3.0/DREAMPlaceFPGA-MP

This specific HPWL and GPT values for each design on MLCAD 2023 benchmark [32] tests based on DREAMPlaceFPGA-MP [30], OpenPARF 3.0 [31], and DrlGo-Design_1-PT are shown in TABLE IX and TABLE X. Compared to DREAMPlaceFPGA-MP, using the pre-trained model DrlGo-Design_1-PT for other design GP optimizations achieved a 13.2% reduction in GPT and a 1.4% reduction in HPWL. Compared to OpenPARF 3.0, DrlGo-Design_1-PT achieved a 2.1% reduction in HPWL and a 1.1% increase in GPT. Therefore, DrlGoFPGA has good scalability on different FPGA architectures, and can still achieve better GP results compared to DREAMPlaceFPGA-MP and OpenPARF 3.0. In TABLE IX and TABLE X, DrlGoFPGA achieved better HPWL values than DREAMPlaceFPGA-MP and OpenPARF 3.0 on 118 and 115 designs (marked in red HPWL values), respectively.

TABLE IX
EXPERIMENTAL RESULTS OF DREAMPLACEFPGA-MP AND DRLGOFPGA (HPWL IN 10^3, GPT in seconds)

Design	DREAMPlaceFPGA-MP [30]		DrlGo-Design_1-PT		Design	DREAMPlaceFPGA-MP [30]		DrlGo-Design_1-PT	
	HPWL	GPT	HPWL	GPT		HPWL	GPT	HPWL	GPT
Design_1	4257.6	34.2	**4145.2**	29.8	Design_120	7209.1	43.9	**7142.7**	40.2
Design_2	4370.1	35.8	**4291.8**	30.9	Design_121	4935.0	34.7	**4860.4**	32.7
Design_5	5755.1	43.9	**4115.3**	36.1	Design_122	4545.2	35.3	**4479.5**	31.3
Design_6	5202.7	34.0	**5185.7**	30.4	Design_125	4908.1	40.0	**4900.4**	36.1
Design_7	5624.6	35.4	**5435.4**	31.4	Design_126	6251.6	34.7	**6156.5**	32.2
Design_10	5754.4	40.3	**5578.3**	36.5	Design_127	5795.6	63.0	**5776.7**	36.1
Design_11	4124.8	35.3	**4092.3**	30.5	Design_130	6308.1	41.0	**6223.3**	37.1
Design_12	4424.7	36.2	**4333.4**	31.9	Design_131	5046.9	35.8	**5010.1**	31.4
Design_15	4046.0	40.9	4067.6	36.4	Design_132	5315.2	37.6	**5093.0**	33.0
Design_16	6150.6	34.0	6206.3	30.2	Design_135	4870.7	40.5	4902.9	37.4
Design_17	6125.2	35.3	**6120.6**	31.9	Design_136	6950.7	35.3	**6863.4**	30.9
Design_20	5851.9	41.3	**5719.1**	37.0	Design_137	7723.0	63.7	**7638.7**	33.3
Design_21	4279.4	35.0	**4176.6**	31.1	Design_140	7815.6	41.0	8061.9	37.7
Design_22	4328.0	37.1	**4275.6**	33.5	Design_141	4610.1	36.7	**4579.6**	32.2
Design_25	4429.8	42.2	**4401.1**	37.6	Design_142	5340.4	37.5	5356.4	34.5
Design_26	5468.0	35.8	**5442.3**	30.9	Design_145	5586.7	43.9	5593.7	39.2
Design_27	5896.2	37.5	**5894.3**	32.5	Design_147	6597.0	37.9	**6448.5**	32.7
Design_30	5784.3	41.4	**5727.6**	37.3	Design_150	6825.6	43.0	6922.4	38.6
Design_31	4516.5	36.4	**4487.1**	31.5	Design_151	5591.5	37.5	**5550.1**	33.1
Design_32	4872.2	37.9	**4829.0**	32.6	Design_152	5791.8	38.2	5810.4	33.8
Design_35	4617.6	42.2	4624.3	38.3	Design_155	4952.4	41.9	4981.2	38.4
Design_36	5966.1	36.3	**5918.2**	31.8	Design_156	6702.7	37.0	**6609.7**	33.7

Design_37	5860.1	37.6	**5773.6**	34.3	Design_160	7429.9	42.7	**7403.3**	38.5
Design_40	6542.7	42.6	**6457.9**	38.0	Design_161	5478.8	36.4	**5467.4**	32.1
Design_41	4440.4	37.0	**4424.3**	32.7	Design_162	5269.7	65.0	**5251.8**	61.0
Design_42	4877.6	38.5	**4778.5**	33.8	Design_165	5366.2	43.5	**5354.9**	39.6
Design_45	4506.7	42.4	**4462.0**	39.0	Design_166	7290.4	63.2	7292.5	58.6
Design_46	6976.5	37.1	6991.3	32.5	Design_167	7472.7	38.7	**7305.8**	34.2
Design_47	6432.7	38.7	**6325.3**	34.0	Design_170	8365.5	44.2	8449.2	40.2
Design_50	6624.4	43.1	**6542.4**	39.4	Design_171	6185.2	37.7	**6030.9**	33.5
Design_51	4925.0	36.4	**4878.1**	33.3	Design_172	6161.8	38.9	**6152.2**	35.3
Design_52	4901.4	37.7	**4868.7**	34.1	Design_175	6004.3	45.2	**5901.7**	41.1
Design_55	5181.0	44.1	**5142.9**	40.6	Design_176	7984.2	37.4	**7846.9**	33.3
Design_56	6186.9	37.0	**6107.0**	33.3	Design_180	6894.0	78.9	**6774.5**	76.9
Design_57	7404.2	38.3	**7307.6**	34.7	Design_181	4026.6	33.8	**3947.3**	31.5
Design_60	6559.2	43.6	**6529.0**	39.7	Design_182	4040.9	34.0	**3920.2**	30.5
Design_61	4172.3	34.5	**4156.5**	30.2	Design_185	4225.5	39.3	**4151.0**	35.7
Design_62	4175.2	36.0	**4087.1**	31.1	Design_186	4993.8	33.9	**4970.8**	32.5
Design_65	4209.5	39.7	4305.2	36.6	Design_187	5703.1	36.0	**5651.1**	32.2
Design_66	6234.6	35.6	**6177.0**	30.1	Design_190	6061.9	40.2	**5968.1**	36.3
Design_67	5572.7	35.6	**5511.5**	30.7	Design_191	3827.8	34.6	3842.5	32.2
Design_70	6197.0	40.5	**5859.2**	36.0	Design_192	4539.3	34.9	**4533.2**	31.6
Design_71	4474.2	35.3	4488.6	31.1	Design_195	3835.9	39.9	3837.6	36.4
Design_72	4497.2	35.5	**4411.1**	31.7	Design_196	5765.5	34.9	5846.0	32.5
Design_75	4264.7	41.0	**4255.4**	36.8	Design_197	5950.6	36.5	**5924.9**	32.2
Design_76	6166.1	35.0	**6152.5**	31.1	Design_200	6005.6	40.5	**5989.3**	36.4
Design_77	6132.5	34.7	**6062.3**	32.1	Design_201	4028.9	35.6	**3961.2**	31.8
Design_80	6131.9	41.2	**5957.4**	36.7	Design_202	4465.4	37.1	**4391.0**	33.1
Design_81	4723.7	35.9	**4792.7**	31.1	Design_205	4344.9	41.9	**4201.4**	37.4
Design_82	5092.1	38.6	**5054.0**	33.1	Design_206	5758.6	34.3	**5528.2**	31.4
Design_85	4698.5	42.0	**4614.3**	37.8	Design_207	5958.8	36.0	**5952.2**	32.6
Design_86	6884.6	36.3	6904.2	31.6	Design_210	5049.5	41.8	**4968.3**	37.6
Design_87	7027.2	35.8	**6660.0**	32.9	Design_211	4538.3	36.3	4575.3	31.6
Design_90	5984.2	41.6	**5938.0**	37.4	Design_212	4687.6	37.4	**4646.8**	33.7
Design_91	5148.7	36.9	**4921.8**	32.0	Design_215	4861.6	42.3	**4831.1**	38.2
Design_92	4593.5	37.2	**4562.6**	32.7	Design_216	5938.7	35.5	**5919.2**	32.2
Design_95	5022.3	42.9	**5006.9**	38.2	Design_217	6230.8	36.8	**6180.3**	32.6
Design_96	5942.0	37.1	**5906.7**	31.0	Design_220	5340.4	42.2	**5333.6**	38.5
Design_97	6435.2	38.1	**6263.3**	33.4	Design_221	4879.5	36.3	**4797.1**	32.4
Design_100	6102.4	42.2	6155.6	38.7	Design_222	4121.3	38.8	**4060.6**	38.7
Design_101	5163.8	37.4	5192.8	32.4	Design_225	4549.7	42.7	**4538.7**	39.2
Design_102	4908.9	38.7	**4773.3**	34.1	Design_226	6718.3	36.0	**6599.7**	32.6
Design_105	5087.7	42.1	**5037.7**	38.9	Design_227	6835.7	38.1	**6689.6**	33.7
Design_106	6834.1	36.8	**6710.3**	32.6	Design_230	6171.3	42.6	**6120.5**	39.0
Design_107	6582.1	37.5	**6565.0**	33.5	Design_231	4728.3	36.8	**4718.8**	33.1
Design_110	8156.8	78.8	**7408.6**	40.0	Design_232	5277.1	38.0	**5228.2**	34.5
Design_111	4946.8	37.6	**4829.4**	33.3	Design_235	5027.9	43.4	**4926.5**	39.8
Design_112	5346.7	38.1	**5296.8**	34.5	Design_236	6534.2	37.1	**6513.2**	33.9
Design_115	5250.0	43.8	**5081.1**	40.1	Design_237	6149.4	38.5	**6083.6**	34.8
Design_116	7601.6	37.7	**7594.9**	34.1	Design_240	5755.1	43.9	**5555.3**	39.7
Design_117	7169.0	38.7	7175.3	34.8					
Overall Ratio						1.014	1.132	1.000	1.000

DrlGo-Design_1-PT：During pre-training model testing, the GO method uses DREAMPlaceFPGA-MP.
The HPWL values marked in red indicate that DrlGo-Design_1-PT achieved better global placement results than DREAMPlaceFPGA-MP.

TABLE X

EXPERIMENTAL RESULTS OF OPENPARF 3.0 AND DRLGOFPGA (HPWL IN 10^3 , GPT in seconds)

Design	OpenPARF 3.0 [31]		DrlGo-Design_1-PT		Design	OpenPARF 3.0 [31]		DrlGo-Design_1-PT	
	HPWL	GPT	HPWL	GPT		HPWL	GPT	HPWL	GPT
Design_1	4571.6	37.0	**4561.8**	38.5	Design_120	7710.6	42.1	7717.7	43.2
Design_2	4628.0	38.9	**4537.2**	38.5	Design_121	5229.8	37.3	5262.8	37.4
Design_5	4373.2	38.5	**4318.4**	38.9	Design_122	4468.4	37.7	**4453.1**	38.1
Design_6	5881.9	37.5	**5840.7**	38.7	Design_125	5497.0	38.1	**5437.1**	39.1
Design_7	6395.9	37.6	**6345.3**	38.8	Design_126	8255.8	37.1	**7782.3**	37.9
Design_10	6632.2	38.0	**6586.4**	38.8	Design_127	7584.9	37.2	**7456.6**	37.8
Design_11	4362.2	39.4	**4340.4**	39.4	Design_130	11982.6	39.0	**8884.0**	39.4
Design_12	4435.9	38.6	4488.1	39.0	Design_131	5691.8	38.9	**5389.4**	39.9
Design_15	4208.7	38.3	**4100.3**	39.1	Design_132	5221.6	39.1	**5152.4**	39.0
Design_16	7537.6	38.7	**7297.7**	39.8	Design_135	5702.7	39.2	**5639.0**	40.3
Design_17	7399.8	39.2	**7162.5**	38.8	Design_136	9376.8	38.6	10812.7	38.3
Design_20	6680.2	39.1	**6575.6**	39.9	Design_137	8830.5	37.3	**8813.2**	38.8

Design_21	4362.0	38.9	**4257.7**	39.7	Design_140	9475.1	37.7	9515.1	38.7
Design_22	4468.7	40.2	**4458.0**	39.9	Design_141	4773.6	39.4	**4760.9**	39.6
Design_25	4610.3	39.9	4651.7	40.7	Design_142	6117.2	39.3	**5984.7**	40.0
Design_26	6265.7	40.4	6344.7	40.7	Design_145	6141.6	40.8	**5978.4**	41.9
Design_27	7038.1	40.6	**6938.0**	41.0	Design_147	8848.7	39.5	**7810.4**	40.1
Design_30	6650.8	39.2	**6608.7**	40.0	Design_150	8116.7	39.1	**8048.3**	39.4
Design_31	4516.5	40.1	**4516.1**	40.5	Design_151	6673.0	40.7	**6481.8**	40.2
Design_32	4994.9	40.2	**4863.4**	40.7	Design_152	13783.8	41.2	**11398.5**	41.8
Design_35	4746.5	40.4	**4716.3**	40.8	Design_155	5539.3	41.3	**5282.1**	42.0
Design_36	7119.8	40.8	**7013.7**	41.4	Design_156	7712.3	40.5	**7702.2**	39.7
Design_37	6624.2	39.1	**6322.9**	40.2	Design_160	8511.5	39.1	**8461.9**	40.2
Design_40	7555.4	39.4	**7399.4**	40.1	Design_161	6742.2	41.2	6905.0	42.4
Design_41	4420.7	39.9	**4400.1**	40.2	Design_162	7583.3	41.8	**7087.2**	41.5
Design_42	4974.0	41.2	**4910.8**	41.3	Design_165	6389.8	41.8	**6388.2**	41.9
Design_45	4669.2	40.8	**4475.1**	41.3	Design_166	7871.6	40.6	**7785.6**	40.3
Design_46	8016.8	41.2	**7976.3**	42.5	Design_167	8149.6	40.1	**8001.3**	41.4
Design_47	6946.7	40.7	6960.7	41.3	Design_170	8669.6	41.0	**8594.2**	41.9
Design_50	7281.2	40.7	7376.0	41.0	Design_171	7223.6	40.8	**6924.0**	40.8
Design_51	5071.8	41.0	**4959.2**	41.7	Design_172	7345.6	41.7	**7069.0**	42.4
Design_52	4707.7	41.0	**4601.5**	42.2	Design_175	6114.8	41.7	6199.1	42.4
Design_55	5104.1	42.4	5233.0	42.5	Design_176	8609.4	41.7	8614.0	41.6
Design_56	6811.6	40.6	**6754.8**	41.4	Design_180	10763.8	43.0	**8989.7**	42.7
Design_57	8108.8	41.0	8114.7	42.0	Design_181	4237.0	37.0	**4135.4**	36.6
Design_60	7410.8	41.7	**7186.6**	42.6	Design_182	4326.2	37.0	**4280.2**	38.8
Design_61	4419.6	37.5	**4179.2**	38.1	Design_185	4682.8	37.4	**4582.2**	38.4
Design_62	4223.6	37.2	**4063.6**	38.4	Design_186	6200.2	36.6	**5985.2**	37.1
Design_65	4390.3	37.9	4422.6	38.3	Design_187	6867.5	37.2	**6764.2**	37.9
Design_66	7009.5	37.8	**6975.8**	38.2	Design_190	7133.8	37.2	7177.7	37.6
Design_67	6508.1	37.6	**6484.0**	37.9	Design_191	4092.0	38.7	**3844.6**	38.3
Design_70	7082.1	38.2	**7071.7**	38.9	Design_192	4862.4	37.7	**4828.3**	37.5
Design_71	4705.0	37.9	**4591.0**	38.7	Design_195	4013.6	38.1	**3976.3**	38.4
Design_72	4706.0	39.0	**4668.0**	40.1	Design_196	6973.5	38.6	**6816.2**	31.2
Design_75	4642.5	39.5	**4400.9**	40.0	Design_197	6970.6	38.3	7039.1	39.6
Design_76	7432.8	38.2	**7270.3**	39.4	Design_200	7449.1	38.8	**7212.7**	38.4
Design_77	7376.8	38.0	**7045.9**	39.0	Design_201	4224.0	39.8	**4167.3**	39.5
Design_80	7383.0	39.4	**7339.2**	39.3	Design_202	4637.0	38.9	**4547.4**	39.5
Design_81	5325.2	39.7	**5078.9**	40.2	Design_205	4620.5	39.3	**4370.8**	40.1
Design_82	5785.1	40.0	**5720.2**	41.0	Design_206	6440.8	39.9	6450.3	39.6
Design_85	4869.9	40.0	**4825.2**	40.4	Design_207	6952.3	38.9	**6928.8**	39.7
Design_86	8112.6	38.3	8518.3	39.1	Design_210	5865.2	39.2	**5800.3**	38.8
Design_87	7956.4	39.4	**7566.4**	39.3	Design_211	4740.8	39.3	**4675.5**	39.8
Design_90	6973.5	39.4	**6858.9**	40.1	Design_212	4940.3	40.1	**4798.7**	39.6
Design_91	5548.8	41.5	**5046.8**	41.4	Design_215	5323.7	40.6	**5284.5**	40.1
Design_92	4640.3	40.0	**4606.1**	40.6	Design_216	6472.8	39.1	6591.5	39.6
Design_95	4865.8	41.0	**4770.9**	41.9	Design_217	6945.0	38.5	**6857.5**	39.5
Design_96	6809.3	39.5	7024.5	40.3	Design_220	6251.9	40.0	**6201.2**	41.4
Design_97	7613.6	40.8	**7429.3**	41.6	Design_221	5124.2	40.5	**4910.3**	40.6
Design_100	9079.7	40.5	**6788.7**	40.5	Design_222	4080.2	39.7	**4079.4**	40.3
Design_101	5899.0	41.8	**5741.0**	41.5	Design_225	4602.5	40.9	**4586.8**	40.7
Design_102	4708.4	41.3	**4695.4**	41.6	Design_226	7454.2	39.3	**7373.4**	40.6
Design_105	5071.3	41.3	5074.3	42.6	Design_227	7539.3	39.6	7355.7	40.6
Design_106	7399.4	39.2	7512.1	40.1	Design_230	6934.4	40.5	**6929.8**	40.6
Design_107	7394.0	39.4	**7306.6**	40.6	Design_231	4840.4	40.5	**4711.6**	40.1
Design_110	7709.3	40.3	**7621.5**	41.7	Design_232	5910.3	41.4	**5802.8**	41.6
Design_111	4583.6	41.4	**4535.6**	42.4	Design_235	5212.3	42.0	5233.7	41.3
Design_112	5795.6	42.5	5946.6	42.8	Design_236	7076.5	40.3	**7064.8**	41.4
Design_115	5073.8	42.2	**5058.5**	43.7	Design_237	6921.5	41.1	**6837.1**	40.6
Design_116	8206.3	40.3	**8193.9**	41.4	Design_240	6356.6	42.0	**6351.9**	42.4
Design_117	7856.3	41.5	**7744.2**	42.6					
Overall Ratio						1.021	0.989	1.000	1.000

DrlGo-Design_1-PT：During pre-training model testing, the GO method uses OpenPARF 3.0.

The HPWL values marked in red indicate that DrlGo-Design_1-PT achieved better global placement results than OpenPARF 3.0.

G. Ablation Study

5) The effect of the parallelizable reward function designed based on the final GP HPWL on solution performance: We studied the effect of different reward function designs on DRL's search for the optimal solution. Fig. 12 shows the experimental results of DrlGoFPGA01-PT on the FPGA01 and using IOBUF HPWL as the reward function. We refer to Maskplace's [13] method of defining the HPWL of macro cells as the reward function to define IOBUF HPWL as the reward function. In Fig. 12, when using IOBUF HPWL as the reward, the return value shows an upward trend with the in-

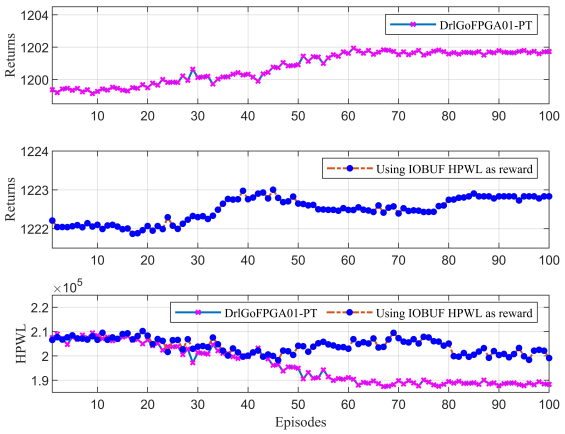

Fig. 12. Comparison of DrlGoFPGA01-PT and using IOBUF HPWL as reward.

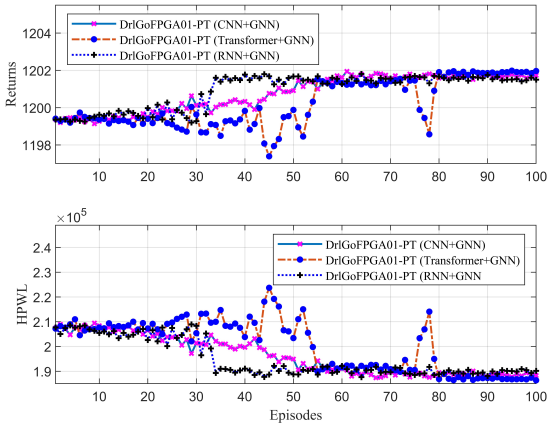

Fig. 13. Comparison of DrlGoFPGA01-PT with different policy network structures.

crease of episodes, while the GP HPWL does not show a significant downward trend. Therefore, having optimal local HPWL values between IOBUFs does not necessarily mean that the GP HPWL is optimal. The HPWL of some macro cells defined by Maksplace is effective because macro cells belong to larger modules in ASICs and have a large number of pins. Having optimal HPWL values between macro cells often leads to better HPWL values. This proves that it is reasonable for this paper to design a parallelizable reward function based on the GP HPWL.

6) The effect of the proposed CNN+GNN policy network structure on solution performance: We investigated the effect of different NNs and GNN combination methods on the optimality and generalization of the IOBUF placement model. Fig. 13 shows the experimental results of DrlGoFPGA01-PT with different policy network structures on FPGA01, including proposed CNN+GNN, Transformer [33]+GNN, and recurrent neural network (RNN) [34]+GNN. TABLE XIII shows the GP results of DrlGoFPGA01-PT on ISPD'2016/2017 benchmarks under different policy network structures. In Fig. 13 and TABLE XIII, the return value of Transformer+GNN reached the highest, and the GP HPWL of FPGA01 during training and testing also reached the minimum, followed by CNN+GNN, and finally RNN+GNN. From the perspective of convergence speed to a stable solution, RNN+GNN can converge to a stable solution faster, while Transformer+GNN is the slowest.

The results in TABLE XIII can be summarized as follows: Compared to CNN+GNN, the GPT of Transformer+GNN and RNN+GNN increased by 3.6% and 2.8% respectively on the ISPD'2016 benchmarks, and were almost the same on the ISPD'2017 benchmarks. The HPWL of Transformer+GNN and RNN+GNN increased by 1.4% and 1.2% respectively on the ISPD'2016 benchmarks, and increased by 1.4% and 0.8% respectively on the ISPD'2017 benchmarks.

Although Transformer+GNN can obtain the optimal pre-trained model, and RNN+GNN can converge to a stable solution faster, the generalization performance of the model is poor. Therefore, the policy network structure, CNN+GNN, designed in this paper has the advantages of obtaining the optimal GP results and better generalization.

TABLE XIII
EXPERIMENTAL RESULTS OF DREAMPLACEFPGA AND DRLGOFPGA ON ISPD'2016/2017 BENCHMARKS (HPWL IN 10^3)

Design	DrlGoFPGA01-PT (Transformer+GNN)		DrlGoFPGA01-PT (RNN+GNN)		Design	DrlGoFPGA01-PT (Transformer+GNN)		DrlGoFPGA01-PT (RNN+GNN)	
	HPWL	GPT (s)	HPWL	GPT (s)		HPWL	GPT (s)	HPWL	GPT (s)
FPGA01	186.5	7.6	189.3	7.4	CLK-FPGA01	1727.8	18.5	1695.2	16.0
FPGA02	488.3	19.9	482.4	18.8	CLK-FPGA02	1745.5	15.8	1710.7	15.9
FPGA03	2057.7	18.8	2071.3	18.5	CLK-FPGA03	4340.8	16.6	4338.7	16.4
FPGA04	4040.4	20.6	4063.0	21.1	CLK-FPGA04	3072.8	15.9	3048.1	15.7
FPGA05	8116.4	20.6	8108.6	21.1	CLK-FPGA05	3909.7	16.8	3827.6	16.9
FPGA06	3339.9	18.9	3358.7	19.2	CLK-FPGA06	4647.3	17.6	4610.7	17.3
FPGA07	6329.3	18.1	6313.9	18.1	CLK-FPGA07	1860.0	17.0	1867.4	16.9
FPGA08	6654.3	20.1	6672.9	19.5	CLK-FPGA08	1614.8	17.6	1609.8	17.9
FPGA09	8259.9	21.7	8178.5	21.2	CLK-FPGA09	1816.1	16.1	1817.5	16.1
FPGA10	3403.8	20.0	3398.4	21.0	CLK-FPGA10	3306.9	16.4	3298.3	16.3
FPGA11	9155.7	20.5	9017.1	20.7	CLK-FPGA11	3121.5	16.0	3116.6	16.0
FPGA12	4511.7	24.5	4428.1	22.4	CLK-FPGA12	2333.0	16.8	2342.1	17.1
Ratio	1.014	1.036	1.012	1.028	CLK-FPGA13	3179.3	16.2	3164.9	16.7
					Ratio	1.014	1.005	1.008	0.994

DrlGoFPGA01-PT: During pre-training model testing, the GO method uses DREAMPlaceFPGA.
Ratio: Calculated based on the experimental results of DrlGoFPGA01-PT (CNN+GNN) in TABLE III and TABLE IV.
DrlGoFPGA01-PT does not support clock routing constraints on ISPD'2017 benchmarks.